#16/Amdt C
4-11-03

501.35437CV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	**M. YOSHIDA et al.**
Application No.:	**09/416,959**
Filed:	**October 13, 1999**
For:	**SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR MANUFACTURING THE SAME**
Art Unit:	**2812**
Examiner:	**R. Pompey**

SUBMISSION OF AMENDMENT UNDER 37 CFR § 1.114

Commissioner for Patents
Washington, D.C. 20231

April 11, 2003

Sir:

In accordance with the provisions of 37 CFR § 1.114, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 42 and 47 as follows:

42. (Twice Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

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a MISFET arranged in said first portion, said MISFET having first semiconductor regions and a gate electrode between said first semiconductor regions;

second semiconductor regions arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;